MoU Activities with SCL, Mohali

Date of execution:
28th October 2015

Name of external agency:

Semi-Conductor Laboratory

Dept of Space, Govt of India

Sector 72, Mohali

Activities conducted:

(2015-16)

1) Prof. J S Ubhi has undergone Internship on CMOS Design and Process Technology, Semi-Conductor Laboratory (SCL), Mohali from December 21, 2015 to January 4, 2016.

2) Prof. J S Ubhi has undergone Internship on CMOS Process Integration and Fabrication Techniques, Semi-Conductor Laboratory (SCL), Mohali from June 06, 2016 to July 05, 2016.

(2016-17)

3) Ms. Rajdevinder Kaur (PEC 1603), Research Scholar undergone 4 to 6 weeks industrial training in SCL, SAS Nagar during June/July 2017.

(2017-18)

4) Three days Workshop on Analog CMOS Integrated Circuit Design was organized by Scientists from SCL, Mohali for faculty, staff and students of SLIET, Longowal during 14th -16th April 2018 (Saturday, Sunday & Monday).

   - Resource Persons: – Er. HS Jatana, Scientist G and Head – Design & Process Group; Semi-Conductor Laboratory (SCL), SAS Nagar, Mohali
   - Er. Ashutosh Yadav, Sci/Engr 'E' ; Semi-Conductor Laboratory (SCL), SAS Nagar, Mohali
   - Er. Rajesh Srivastava, Sci/Engr 'D' ; Semi-Conductor Laboratory (SCL), SAS Nagar, Mohali


Three Days' Workshop
on
Analog CMOS Integrated Circuit Design
April 14-16, 2018


Three Days' Workshop
on
Analog CMOS Integrated Circuit Design

(2018-19)

5) Mr. Mukesh Kumar, Research scholar (ECE) visited SCL, Mohali for his Ph.D. work from 09/10/2019 to 01/11/2019 for the purpose of using laboratory facility and discussions related to research activity.

6) Er. H S Jatana, Group Head-DPG, SCL Mohali, Chandigarh delivered experts talks on November 8th, 2019, on following topics during STC on "Nanoelectronics & VLSI: Devices, Circuits & Systems" organized from Nov. 4-8, 2019 under twinning activities with NIT, Srinagar Garhwal:

- Analog Design-Front end and
- Challenges & Issues in design of SOCs 8-11-2019

(2020-21)

7) Prof. J S Ubhi and Mr. Mukesh Kumar has published following SCI paper with Scientists from SCL, Mohali

   - Mukesh Kumar, Jagpal Singh Ubhi, Sanjeev Basra, Anuj Chawla, H.S. Jatana, "Total ionizing dose hardness analysis of transistors in commercial 180 nm CMOS technology" Microelectronics Journal, Volume 115, 105182, 2021 (Impact factor 1.605)

(2022-23)

8) Expert talk on "Recent Trends Semiconductors and Electronics" held on 24.01.2023 during 9.30am 11.30am by Er. HS Jatana Ex Scientist G, Semiconductor Complex Laboratory, Mohali for Faculty, staff and students of UG/PG/PhD program.

Activities planned:

Joint Research Project/PhD guidance