MEMORANDUM OF UNDERSTANDING

BETWEEN



SEMI-CONDUCTOR LABORATORY, DEPARTMENT OF SPACE, GOVT. OF INDIA S.A.S. NAGAR

AND



SANT LONGOWAL INSTITUTE OF ENGINEERING & TECHNOLOGY LONGOWAL, DISTRICT SANGRUR

FOR

COLLABORATION ON RESEARCH & DEVELOPMENT, FACULTY AND STUDENT EXCHANGE

MEMORANDUM OF UNDERSTANDING FOR COLLABORATION ON RESEARCH & DEVELOPMENT, FACULTY AND STUDENT EXCHANGE

In furtherance of their mutual interest in the fields of education and research and as a contribution towards increasing national cooperation, Semi-conductor Laboratory, Department of Space, Government of India having its registered address at Sector 72, S.A.S. Nagar – 160071, Punjab, India (hereinafter referred to as SCL)

and

Sant Longowal Institute of Engineering & Technology having its registered address at Longowal – 148106 District Sangrur, Punjab, India (hereinafter referred to as SLIET) have entered into this Memorandum of Understanding (MoU) on this 28th day of October 2015 with broad terms and conditions as follows:

ARTICLE - I

The MoU involves collaboration between SCL and SLIET (both also referred to as institution) in related disciplines.

The two institutions shall seek to promote:

- 1. Exchange of staff and students (faculty, research scholars, M.Tech students, B.Tech students and research project employees) regarding academics and research for mutual benefit of both institutions.
- 2. Exchange of students for pursuing course study and academic programmes for mutual benefit of both institutions.
- 3. Collaboration in teaching, research & development and consultancy activities.
- 4. Exchange of academic and research material and publications/IPs.
- 5. Cooperation in project proposals and research activities of mutual interest.
- 6. Provision of cultural and intellectual enrichment opportunities for staff and students of both institutions.

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- 7. Collaboration in research & development in the areas of (i) Advanced VLSI Device Fabrication, (ii) MEMS Fabrication, (iii) VLSI Device/MEMS Characterization, (iv) VLSI/CMOS-RF Circuit Design and (v) VLSI Device Modeling at both SLIET and SCL. This also includes collaboration in setting-up and upkeep of the relevant infrastructure in both the institutions.
- 8. Joint publication of research papers in international scientific journals and in conferences in case of supervision from both institutions.
- 9. Exchange of students for summer/winter internships
- 10. Publication of Intellectual Properties (IPs) developed jointly through project/research collaboration. Such IP would acknowledge joint inventorship of personnel/students belonging to both the institutions, as applicable.
- 11. Writing books/booklets jointly in the areas listed above or in any other area of mutual interest.

ARTICLE - II

The activities under this MoU will include:

1. Staff Exchange

- Staff exchange activities cover visits to either institution for any of the following purposes:
- (i) Undertaking joint research
- (ii) Attachment of staff for purposes of curriculum development and review, attendance in courses and upgrading of teaching and research skills
- (iii) Participation in seminars, colloquia and other types of academic discussions
- (iv) Contributions to teaching programmes
- (v) Co-supervision of M.Tech and Ph.D students
- (vi) Conduct study tours
- (vii) Research and joint consultancy work
- (viii) Facilitation for higher studies (M.Tech and Ph.D) for Department of Space / SCL employees at SLIET

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2. Student Exchange:

Student exchange activities (for B.Tech/M.Tech/Ph.D students) cover visits to either institution for any of the following purposes:

- Participation in research (i)
- Internships of 2-12 months duration for SLIET students at SCL (ii)

3. Exchange of Academic Materials

Exchange of relevant academic materials will be carried-out subject to mutual agreement of the institutions.

ARTICLE - III

Implementation of cooperation based on this MoU shall be dealt with between the relevant faculties and divisions/departments of both institutions. Wherever necessary and subject to availability of resources, a specific plan shall be worked-out for each activity mentioned above in Article - I & II setting forth detailed arrangements for collaboration. Such plans shall be subject to approval of the appropriate authorities of each institution. To facilitate development of such plans, each institution shall nominate a member of its staff to coordinate activities arising under this MoU.

ARTICLE - IV

Both institutions agree and undertake to keep confidential, at all times, any information and/or data that may be exchanged, acquired and/or shared in connection with the area of cooperation as mentioned above in ARTICLE - I (3) unless otherwise the same information already exists in the public domain.

ARTICLE - V

Ownership of any research findings shall be vested with both institutions in this MoU and any publications regarding the same shall only be possible after prior approval from both the institutions.

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ARTICLE - VI

The MoU shall remain in force for a period of 10 (TEN) years commencing from the date of signing and may be reviewed/renewed by mutual consent by serving 3 (Three) months written notice to the other institution. The MoU may be amended with mutual consent of both the institutions in writing.

ARTICLE - VII

Both SCL and SLIET reserve the right to terminate this MoU by either institution giving 3 (Three) months written notice to the other. Where such termination occurs, the provisions of this MoU shall continue to apply to ongoing activities until their completion.

ARTICLE - VIII

Participating staff and students involved in any activities under this MoU must adhere to laws of the country and rules & regulations of the host institutions.

ARTICLE - IX

SCL and SLIET welcome establishment of this MoU for cooperation and jointly agree to the provisions as set-out above. There will be two copies of this MoU equally valid, one for each institution, effective from the date of its signing.

Semi-conductor Laboratory

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Surinder Singh Director

सुरिन्दर सिंह / Surinder Singh निरेशक / Director सेनी - कंडबरर लेबोरेटरी Semi-Conductor Laboratory कवित्व विषय, पारस सरकार Department of Space, Govt. of India श्रिस्टर-72, स.स. से. नगर-160071, पंजाब, भारत Sector-72, S.A.S. Nagar-160071, Punjab, INDIA

Witness SBhatragas

ant प्रमाण SANDAY BHATHAGAR Date: जा जान परियोजना शियोजन हुव Date: जान Head Protect Planning Group Sant Longowal Institute of Engg. & Tech.

The am 15/15

Prof. V K Jain Director

Witness (Inf. M. B. BEF Dean (Acd) Date: 2.8./....